In the Claims

The following is a marked-up version of the claims with the language that is underlined ("___") being added and the language that contains strikethrough ("—") being deleted:

1. (Currently amended) A memory device, comprising:

a plurality of memory blocks each having at least two nodes;

a plurality of odd and even repeaters arranged in an alternating configuration with the memory blocks such that each memory block is positioned between an odd and even repeater pair, the repeaters being configured to repeat both a control signal and a drive voltage; and

a line that couples the memory blocks with the repeaters ~~such that the repeaters can read from the memory blocks~~.

2. (Original) The device of claim 1, wherein the memory blocks are magnetic random access memory (MRAM) blocks.

3. (Original) The device of claim 1, wherein the repeaters are configured to sense whether the line is selected, and if the line is selected, provide a voltage to the line.

4. (Original) The device of claim 1, wherein the line is configured by coupling word lines of the memory blocks to each other, a word line of one of the memory blocks having a same address as addresses of word lines of remaining memory blocks.

5. (Currently amended) The device of claim 1, wherein the line couples a decoder, the repeaters, and the memory blocks, and wherein the memory blocks are in series with the repeaters and the decoder~~, and wherein a repeater is located adjacent to each memory block~~.

6. (Original) The device of claim 1, wherein a repeater comprises a comparator, access transistors, and at least one drive transistor, and wherein a repeater is configured to sense voltage at an output of each memory block, and to provide a voltage to each node of the line.

7. (Currently amended) A memory device, comprising:

a plurality of memory blocks each having at least two nodes;

a plurality of odd and even repeaters arranged in an alternating configuration with the memory blocks such that each memory block is positioned between an odd and even repeater pair, one of the repeaters of each repeater pair providing a high voltage to a memory block node and the other providing a low voltage to another memory block node during a write process; and

a line that couples the memory blocks to the repeaters such that the repeaters can write to the memory blocks.

8. (Original) The device of claim 7, wherein the memory blocks are magnetic random access memory (MRAM) blocks.

9. (Currently amended) The device of claim 7, wherein at least one repeater of the repeater pair is configured to sense an output of ~~each~~ an associated memory block and provide a voltage to the ~~output~~ memory block.

10. (Original) The device of claim 7, wherein the line couples a decoder, the repeaters and the memory blocks, the memory blocks are in series with the repeaters and the decoder, and wherein a repeater is located adjacent to each memory block.

11. (Currently amended) A method for communicating with a selected memory blocks of a memory device that includes a plurality of memory blocks, comprising:

coupling the selected memory blocks to a pair odd and even repeaters; and

~~reading from~~ writing to the selected memory blocks by providing a high voltage to the selected memory block with one of the odd and even repeaters and providing a low voltage to the selected memory block with the other of the odd and even repeaters.

12. (Currently amended) The method of claim 11, wherein the memory blocks of the memory device are magnetic random access memory (MRAM) blocks.

13-27. (Cancelled)

28. (New) The method of claim 11, wherein writing to the selected memory block comprises repeating a control signal and a drive voltage using one of the repeaters of a pair of odd and even repeaters.